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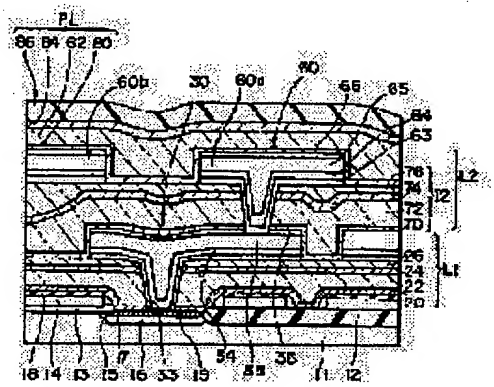
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device with improved reliability and device characteristics having a protecting insulating film and manufacturing method thereof, by improving the flatness and reducing the interlayer capacity.
SOLUTION: A semiconductor comprises a semiconductor substrate 11, a plurality of wiring regions L1, L2 formed on the semiconductor substrate 11, and a protecting insulating film PL formed on the wiring region located in the uppermost layer from between the wiring regions L1, L2. The protecting insulating film PL comprises a first silicon oxide film 80, a second silicon oxide film 82 formed on the first silicon oxide film 80 and formed by polycondensation reaction between a silicon compound and hydrogen peroxide, and a silicon nitride film 86 constituting the uppermost layer.



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CLAIMS

[Claim(s)]
[Claim 1] The protection insulator layer formed on the wiring field located in the best layer of two or more wiring fields formed on the semiconductor substrate containing an element and the aforementioned semiconductor substrate and these wiring fields is included. The aforementioned protection insulator layer is a semiconductor device containing the 2nd silicon oxide which was formed on the 1st silicon oxide and the 1st silicon oxide of the above, and was formed of the polycondensation reaction of a silicon compound and a hydrogen peroxide, and the silicon nitride which constitutes the best layer.
[Claim 2] The semiconductor device which has the 3rd porous silicon oxide on the 2nd silicon oxide of the above further in a claim 1.
[Claim 3] The 1st silicon oxide of the above is a semiconductor device whose thickness is 50-500nm in a claim 1 or a claim 2.
[Claim 4] The 2nd silicon oxide of the above is a semiconductor device which has the thickness with which the concavo-convex best side where thickness is constituted in either a claim 1 or the claim 3 by the 1st silicon oxide of the above is covered.
[Claim 5] The aforementioned silicon nitride is a semiconductor device whose thickness is 300-1500nm in either a claim 1 or the claim 4.
[Claim 6] The process which is the manufacture method of the semiconductor device containing the protection insulator layer formed on the wiring field located in the best layer of two or more wiring fields formed on the semiconductor substrate containing an element and the aforementioned semiconductor substrate and these wiring fields, and forms the aforementioned protection insulator layer is the manufacture method of the semiconductor device which contains following process (a) - (d) at least.
(a) The process which at least one sort of a silicon compound and the compound containing oxygen and oxygen is made to react by the chemical-vapor-deposition method, and forms the 1st silicon oxide, the process which the (b) silicon compound and a hydrogen peroxide are made to react by the chemical-vapor-deposition method, and forms the 2nd silicon oxide, the process which performs annealing processing at (c)350-500 degree C temperature, and the process which forms (d) silicon nitride.
[Claim 7] The manufacture method of a semiconductor device including the process (e) which the compound containing at least one sort and impurity of the compound containing a silicon compound, oxygen, and oxygen is made to react by the chemical-vapor-deposition method, and forms the 3rd porous silicon oxide after the aforementioned process (b) in a claim 6.
[Claim 8] the silicon compound used at the aforementioned process (b) in a claim 6 or a claim 7 — a mono silane, a disilane, and SiH2 — the manufacture method of the semiconductor device which is at least one sort chos n from organic silane compounds, such as inorganic silane compounds, such as Cl2, SiF4, and CH3SiH3, and a TORIPURO pill silane, and a tetrapod ethoxy silane
[Claim 9] The aforementioned process (b) is the manufacture method of the semiconductor device which the aforementioned silicon compound is an inorganic silane compound in either a claim 6 or the claim 8, and is performed by the reduced pressure chemical-vapor-deposition

method under 0-20-degree C temperature conditions.
[Claim 10] The aforementioned proc ss (b) is the manufacture method of the semiconductor device which the aforementioned silicon compound is an organic silane compound in either a claim 6 or the claim 8, and is performed by the reduced pressure chemical-vapor-deposition method under 100-150-degr C temperature conditions.
[Claim 11] It is the manufacture method of a semiconductor device that the aforementioned process (a) is performed by the plasma-chemistry vapor growth under 300-500-degree C temperature conditions in either a claim 6 or the claim 10.
[Claim 12] The silicon compound used at the aforementioned process (a) in either a claim 6 or the claim 11 is the manufacture method of the semiconductor device which is an organic silane compound.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the semiconductor device which has the protection insulator layer formed on the metal wiring which turned minutely below into the half micron, and its manufacture method about a semiconductor device and its manufacture method.
[0002]
Background of the Invention] On the metal wiring layer of the best layer of the semiconductor device used for LSI etc., in order to prevent the invasion of a physical injury and contamination, or moisture, the protection insulator layer is formed. Generally as a protection insulator layer, the silicon nitride which carried out the plasma vapor growth, for example at low temperature is used. Moreover, what has the laminated structure which formed the silicon oxide for stress relief in the lower layer of a silicon nitride as a protection insulator layer is used. It consists of the silicon oxide which was made to carry out the vapor growth of a mono silane, oxygen, or the dinitrogen oxide, and was formed as a protection insulator layer which has such a laminated structure, a PSG (phosphorus glass) film which doped Lynn to this or an SOG (spin ON glass) film, and a silicon nitride which was formed of the plasma-chemistry vapor growth using a mono silane, ammonia, or nitrogen gas and whose thickness is about 1 micrometer.
[0003] This protection insulator layer uses a photoresist as a mask, and selective etching is carried out by dry etching or wet etching, and it has opening for constituting the bonding putt section for external electrode ejection.
[0004] By the way, in processing by etching of a metal wiring layer, when a semiconductor device turns minutely into below submicron one, since anisotropy dry etching is adopted, the side-attachment-wall section of a metal wiring layer has an almost perpendicular steep inclination. And the silicon oxide and silicon nitride which constitute a protection insulator layer are attached by the dregs ping, and since the surroundings are bad, a void is easy to be formed in the specific space of a metal wiring layer. The portion of this void serves as a contamination trap. Moreover, in the corner of the side-attachment-wall section of a metal wiring layer, and a slot, since a silicon nitride becomes [the thickness] very thin compared with a flat part, moisture and contamination tend to invade from a portion with this thin thickness, and there is a problem in respect of reliability over a long period of time.
[0005] Furthermore, in order to raise the working speed of a device, reduction of the capacity between layers is needed, and at the former, it is ********** about cautions to the capacity between layers between a metal wiring layer, a substrate, or the wiring layer of the vertical direction. However, with the structure of a protection insulator layer where contribution of a lateral capacity between layers becomes large by detailed-ization of a wiring space, therefore a silicon nitride with a high dielectric constant exists between the spaces between metal wiring in the same layer, a lateral capacity between layers has not ignored the point on electrical properties, such as a working speed.
[0006]
[Problem(s) to be Solved by the Invention] The purpose of this invention is to offer the

semiconductor device which has the protection insulator layer which can contribute to improvement in reliability and a device property by the improvement of flat nature, and reduction of the capacity between layers, and its manufacture method.
[0007]
[Means for Solving the Problem] The manufacture method of the semiconductor device of this invention is the manufacture method of the semiconductor device containing the protection insulator layer formed on the wiring field located in the best layer of two or more wiring fields formed on the semiconductor substrate containing an element, and the aforementioned semiconductor substrate, and these wiring fields, and the process which forms the aforementioned protection insulator layer contains following process (a) – (d) at least.
[0008] (a) The process which at least one sort of a silicon compound and the compound containing oxygen and oxygen is made to react by the chemical–vapor–deposition method, and forms the 1st silicon oxide, the process which the (b) silicon compound and a hydrogen peroxide are made to react by the chemical–vapor–deposition method, and forms the 2nd silicon oxide, the process which performs annealing processing at (c)350–500 degree C temperature, the process which forms (d) silicon nitride.
[0009] According to the manufacture method of this semiconductor device, the layer which was excellent in flat nature can be formed at low temperature by making a silicon compound and a hydrogen peroxide react by the chemical–vapor–deposition method, and forming the 2nd silicon oxide according to a process (b). That is, the 2nd silicon oxide formed at this process (b) has the self–flattening property of having a high fluidity and having excelled in itself. If the mechanism makes a silicon compound and a hydrogen peroxide react by the chemical–vapor–deposition method, it will be considered to be because for a silanol to be formed into a gaseous phase, and for a fluid good film to be formed when this silanol deposits on a wafer front face.
[0010] For example, when a mono silane is used as a silicon compound, a silanol is formed at the reaction shown by the following formula (1), (1)', etc.
[0011] Formula (1)
SiH4+2H2O2 -> Si(OH)4+2H2 formula (1) The silanol formed by 'SiH4+3H2O2 -> Si(OH)4+2H2 O+H2 and the formula (1), and (1)' serves as a silicon oxide, when water ****s at the polycondensation reaction shown by the following formula (2).
[0012] Formula (2)
Si (OH)4 -> as the SiO2+2H2O aforementioned silicon compound — a mono silane, a disilane, and SiH2 — organic silane compounds, such as inorganic silane compounds, such as Cl2, SiF4, and CH3SiH3, and a TORIPURO pill silane, and a tetrapod ethoxy silane, etc. can be illustrated
[0013] Moreover, under 0–20–degree C temperature conditions, when the aforementioned silicon compound is an inorganic silicon compound, when the aforementioned silicon compound is an organic silicon compound, it is desirable [the membrane formation process of the aforementioned process (b)] to be carried out by the reduced pressure chemical–vapor–deposition method under 100–150–degree C temperature conditions. If temperature is higher than the aforementioned upper limit, when the polycondensation reaction of the aforementioned formula (2) progresses too much, the 1st silicon oxidization membrane fluidity will become low, and good flat nature will be hard to be obtained at this membrane formation process. Moreover, there is un–arranging [to which adsorption of a low and the decomposition moisture within a chamber and dew condensation out of a chamber occur, and it becomes difficult from the aforementioned lower limit for membrane formation equipment to control temperature].
[0014] As for the 2nd silicon oxide formed at the aforementioned process (b), it is desirable to be formed by the thickness of the grade which can fully cover the level difference of a wafer substrate front face, i.e., sufficient thickness to cover the best side of the irregularity constituted by the 1st silicon oxide located under this 2nd silicon oxide. The thickness of the 2nd silicon oxide is 500–1000nm preferably, although the lower limit is dependent on the height of the irregularity of the 1st silicon oxide under the 2nd silicon oxide. When the thickness of the 2nd silicon oxide exceeds the aforementioned upper limit, a crack may be produced for the stress of the film itself.
[0015] In this invention, before the aforementioned process (b), at least one sort of a silicon

compound and the compound containing oxygen and oxygen is made to react by the chemical-vapor-deposition method, and the 1st silicon oxide used as a base layer is formed. This base layer has from it the passivation function which neither moisture nor an excessive impurity moves from the 2nd silicon oxide of the above, and the function which raises the adhesion of the 2nd silicon oxide in a lower layer.

[0016] It is desirable to include the process (e) which the compound containing at least one sort and impurity of the compound containing a silicon compound, oxygen, and oxygen is made to react by the chemical-vapor-deposition method, and forms the 3rd porous silicon oxide on the 2nd silicon oxide of the above after the aforementioned process (b).

[0017] This 3rd silicon oxide is porosity and it not only functions as a cap layer, but can emit gradually outside the gas constituents generated from the 2nd silicon oxide in annealing processing of a next process (c). Furthermore, in addition to being porosity, this 3rd silicon oxide can ease the stress of this film by weakening the bonding strength between Si-O molecules of impurities, such as Lynn and boron, and the silicon oxide which constitutes this film by adding Lynn preferably on this film, and can constitute the layer which cannot break soft further easily moderately so to speak. The concentration of the impurity contained in the 3rd silicon oxide is 1 - 6 % of the weight preferably, when the point of the stress relaxation of the film mentioned above is taken into consideration.

[0018] Moreover, since the 3rd silicon oxide has the compression stress of 100-600MPa, in case the 2nd silicon oxide carries out a polycondensation, it has the function to prevent that **** stress increases and a crack enters. Furthermore, the 3rd silicon oxide also has the function to prevent moisture absorption of the 2nd silicon oxide.

[0019] As for the aforementioned process (e), it is desirable to be carried out under 300-450-degree C temperature conditions by the plasma-chemistry vapor growth by the RF 1MHz or less. By forming membranes on this temperature condition, it becomes easy to escape by the annealing initial stage by annealing of a process (c) from gas constituents, and the reliability of a device improves.

[0020] Moreover, as for the compound containing oxygen used at the aforementioned process (e), it is desirable that it is a dinitrogen oxide (N2O). Since the dinitrogen oxide of the plasma state tends to react by using a dinitrogen oxide as reactant gas with the hydrogen bond (-H) of the silicon compound which constitutes the 2nd silicon oxide, while forming the 3rd silicon oxide, desorption of the gasification component (hydrogen, water) of the 2nd silicon oxide can be promoted.

[0021] The aforementioned process (e) may be performed by the ordinary-pressure chemical-vapor-deposition method under 300-500-degree C temperature conditions instead of a plasma-chemistry vapor growth. In this case, as for the compound containing the aforementioned oxygen used at the aforementioned process (e), it is desirable that it is ozone.

[0022] Furthermore, before forming the 2nd silicon oxide of the above at the aforementioned process (e), it is desirable to expose the 2nd silicon oxide of the above to ozone atmosphere. Since ozone tends to react by passing through this process with the hydrogen bond (-H) of a silicon compound and the hydroxyl group (-OH) which constitute the 2nd silicon oxide, the hydrogen in the 2nd silicon oxide and desorption of water can be promoted.

[0023] Moreover, the thickness of the 3rd silicon oxide is 100nm or more preferably, when the point of flat nature and a crack is taken into consideration.

[0024] At the aforementioned process (c), by performing annealing processing at the temperature of 350-500 degrees C, the 2nd and 3rd silicon oxides formed by the aforementioned process (b) and (e) turn precisely, and its moisture resistance improves in an insulating row.

[0025] That is, if it sees about the 2nd silicon oxide, in the early stages of this annealing processing, the polycondensation reaction by the formula (2) mentioned above will be completed, water and hydrogen which are produced with this reaction will be emitted outside through the hole of the 3rd silicon oxide, and the 2nd silicon oxide will be precisely formed, where a gasification component is fully removed. Moreover, the 3rd silicon oxide turns into a precise film from porosity by annealing processing.

[0026] In this annealing processing, the 2nd and 3rd silicon oxides can be made precise enough

by making temperature into 350 degrees C or more. Moreover, if an annealing temperature is performed at the temperature exceeding 500 degrees C, the metal wiring layer which consists of a metal or alloys, such as aluminum, will become easy to receive a heat damage.
[0027] Moreover, by forming the 3rd porous silicon oxide on the 2nd silicon oxide Even if there is a rapid temperature change in annealing processing at a process (c) like [at the time of putting a wafer directly on the bottom of the temperature of 350-500 degrees C], in order for the 3rd silicon oxide of the above to have moderate softness and to control discharge of rapid moisture, Annealing processing can be performed without producing a crack in this 2nd silicon oxide, since the stress of the 2nd silicon oxide is absorbable.
[0028] furthermore, annealing processing of the aforementioned process (c) — continuing — a process (d) — a chemical-vapor-deposition method — a silicon nitride is preferably formed by the plasma-chemistry vapor growth This silicon nitride has 300-1500nm thickness preferably, when moisture resistance and resistance to contamination are taken into consideration.
[0029] In the manufacture method concerning this invention, flattening is fully attained by the 1st silicon oxide and the 2nd silicon oxide. Consequently, the silicon nitride of the best layer is attached, the surroundings are good, there are few the portions and the defects which thickness is thin, locally, and moisture resistance and resistance to contamination can aim at improvement in the reliability as a protective coat highly.
[0030] The semiconductor device formed by the above manufacture method The protection insulator layer formed on the wiring field located in the best layer of two or more wiring fields formed on the semiconductor substrate containing an element and the aforementioned semiconductor substrate and these wiring fields is included. The aforementioned protection insulator layer contains the 2nd silicon oxide which was formed on the 1st silicon oxide and the 1st silicon oxide of the above, and was formed of the polycondensation reaction of a silicon compound and a hydrogen peroxide, and the silicon nitride which constitutes the best layer.
[0031] Since according to this semiconductor device the mutual space of the wiring layer which it not only has reliability high as a protection insulator layer, but adjoins in the metal wiring layer of the best layer is filled up with a silicon oxide with a low dielectric constant as mentioned above, the influence of a silicon nitride with a high dielectric constant can be small, and can improve a working speed compared with the conventional structure.
[0032] As for the silicon oxide which the silicon compound and hydrogen peroxide which are formed at the aforementioned process (b) and the same process are made to react by the chemical-vapor-deposition method, and is obtained, in this invention, it is desirable to apply also to the flattening layer of the mutual layer insulation film of a metal wiring layer at the layer insulation film formed on the semiconductor substrate containing elements, such as a MOS device, and a row.
[0033]
[Embodiments of the Invention] Drawing 1 - drawing 5 are the outline cross sections for explaining the manufacture method of the semiconductor device concerning this invention, and the form of 1 operation of a semiconductor device. Drawing 1 (A) - (C) and drawing 2 (A), and (B) show the process for drawing 3 (A), (B) and drawing 4 (A), and (B) manufacturing the wiring field L2 of the 2nd layer, and drawing 5 manufacturing the protection insulator layer of multilayer structure for the wiring field L1 of the 1st layer.
[0034] Below, an example of the manufacture method of a semiconductor device is shown.
[0035] (A) Explain the process shown in drawing 1 (A).
[0036] (Formation of an element) The MOS device is formed in a silicon substrate 11 by the method generally used first. Specifically, the field insulator layer 12 is formed of selective oxidation on a silicon substrate 11, and the gate oxide film 13 is formed in an active field. The gate electrode 14 is formed by carrying out the spatter of the tungsten silicide on the polysilicon contest film into which SiH4 was pyrolyzed and was grown up, carrying out the laminating of the silicon oxide 18 further, and **********ing to a predetermined pattern further by channel pouring, after adjusting threshold voltage. At this time, the wiring layer 37 which consists of a polysilicon contest film and a tungsten silicide film is formed on the field insulator layer 12 if needed.

[0037] Subsequently, the low concentration impurity layer 15 of a source field or a drain field is formed by carrying out the ion implantation of Lynn. Subsequently, after the side-attachment-wall spacer 17 which becomes the side of the gate electrode 14 from a silicon oxide is formed, the high concentration impurity layer 16 of a source field or a drain field is formed by carrying out the ion implantation of the arsenic and activating an impurity by annealing processing using the halogen lamp.
[0038] Next, a predetermined silicon-substrate field is exposed by forming a vapor-growth silicon oxide 100nm or less, and **********ing this film alternatively with the mixed-water solution of HF and NH4F. then — for example, the silicon-substrate front face which carried out opening by carrying out the spatter of the titanium by about 30-100nm thickness, and performing moment annealing for several seconds - about 60 seconds at the temperature of 650-750 degrees C into the nitrogen-gas-atmosphere mind which controlled oxygen to 50 ppm or less — the monochrome silicide layer of titanium — a silicon-oxide 18 top — titanium — a rich titanium night RAIDO (TiN) layer is formed Subsequently, if immersed into NH4OH and the mixed-water solution of H2O2, etching removal of the aforementioned titanium night RAIDO layer will be carried out, and the monochrome silicide layer of titanium will remain only in a silicon-substrate front face. Furthermore, perform 750-850-degree C lamp annealing, the aforementioned monochrome silicide layer is made to form into die silicide, and the titanium silicide layer 19 is formed in the front face of the high concentration impurity layer 16 at a self-adjustment target.
[0039] In addition, when the gate electrode 14 is formed only with contest polysilicon and it is made to expose by selective etching, both a gate electrode, source, and drain field become the CHITANSARI side structure separated with the side-attachment-wall spacer.
[0040] In addition, the Salicide structure may consist of tungsten silicide and molybdenum silicide instead of titanium silicide.
[0041] (B) Next, explain the process shown in drawing 1 (B).
[0042] (Formation of the 1st layer insulation film I1) The 1st layer insulation film I1 consists of the 1st silicon oxide 20, the 2nd silicon oxide 22, the 3rd silicon oxide 24, and the 4th silicon oxide 26 in order of the silicon oxide of four layers, i.e., a lower shell.
[0043] a. **** of the 1st silicon oxide 20 — the 1st silicon oxide 20 of 100-200nm of thickness is first formed by making a tetrapod ethoxy run (TEOS) and oxygen react by the plasma-chemistry vapor-growth (CVD) method at 300-500 degrees C This silicon oxide 20 does not have oxidization or the dregs ping of the silicide layer 19, either, and highly [insulation], its etch rate to the solution of hydrogen fluoride is also slow, and it turns into a precise film from the film grown up from SiH4.
[0044] Since a oxidizing gas and titanium silicide will tend to produce a crack and exfoliation simply in response to the early stages of membrane formation here if the membrane formation temperature at this time is high although the direct silicon oxide 20 is made to form on the titanium silicide layer 19, as for processing temperature, it is preferably desirable to carry out at 250-400 degrees C more preferably 600 degrees C or less. And if it is annealing and vapor-phase-oxidation processing which are exposed to oxidizing atmospheres other than a steam after [which the silicon oxide mentioned above in about 100nm thickness on the titanium silicide layer 19] being comparatively formed at low temperature, it will not become a problem even if it raises temperature to 900-degree-C grade.
[0045] b. Form the 2.5x102Pa or less of the 2nd silicon oxide 22 preferably formation of the 2nd silicon oxide 22, next by making SiH4 and H2O2 react by CVD by using nitrogen gas as a carrier more preferably under reduced pressure of O.3x102 to 2.0x102Pa. The 2nd silicon oxide 22 is formed by the thickness which has larger thickness than the level difference of the 1st lower layer silicon oxide 20 at least, that is, fully covers this level difference. Moreover, the upper limit of the thickness of the 2nd silicon oxide 22 is set as the grade which a crack does not produce in this film. Specifically, in order to obtain better flat nature, as for the thickness of the 2nd silicon oxide 22, it is desirable that it is thicker than a lower layer level difference, and it is preferably set as 300-1000nm.
[0046] Since it participates in the fluidity at the time of membrane formation of this film, membrane fluidity will fall if membrane formation temperature is high, and the membrane

formation temperature of the 2nd silicon oxide 22 spoils flat nature, 0–20 degrees C of temperature at the time of membrane formation are more preferably set as 0–10 degrees C.
[0047] Moreover, although especially the flow rate of H2O2 is not restricted, it is desirable that it is a flow rate more than the double precision of SiH4, and it is desirable to be set as the flow rate range of 100 – 1000SCCM by gas conversion from membranous homogeneity and the point of a throughput.
[0048] The 2nd silicon oxide 22 formed at this process is in the state of silanol polymer, and a fluidity is good and has a high self–flattening property. Moreover, since many hydroxyl groups (–OH) are included, the 2nd silicon oxide 22 has hygroscopicity in a high state.
[0049] c. Put under existence of formation of the 3rd silicon oxide 24 next SiH4 and PH3, and N2O, and it is at the temperature of 300–450 degrees C. By making gas react by the plasma CVD method by 200–600kHz high frequency, the PSG film (the 3rd silicon oxide) 24 of 100–600nm of thickness is formed. As for this 3rd silicon oxide 24, it is desirable to be formed after being saved in the atmosphere in which the hygroscopicity of the 2nd silicon oxide 22 of the above is continuously formed in in consideration of a high thing following formation of the 2nd silicon oxide 22 of the above, or the 2nd silicon oxide 22 does not contain moisture.
[0050] Moreover, the 3rd silicon oxide 24 needs that desorption of gasification components, such as water contained in the 2nd silicon oxide 22 of the above by the annealing processing performed behind and hydrogen, is easy, and to be porous (porosity) in consideration of fully being carried out. For that purpose, temperature is desirable and it is preferably [more] desirable [the 3rd silicon oxide 24] 1MHz or less preferably to form membranes by the 200–600kHz plasma CVD method more preferably, and to include impurities, such as Lynn, 300–400 degrees C 450 degrees C or less. By containing such an impurity in the 3rd silicon oxide 24, it will be in a more nearly porous state and the 3rd silicon oxide 24 not only can ease the stress to a film, but can have the gettering effect over alkali ion etc. with it. The concentration of such an impurity is set up in consideration of points, such as the gettering effect. For example, when an impurity is Lynn, it is desirable to be contained at 2 – 6% of the weight of a rate.
[0051] Moreover, in plasma CVD, desorption of the hydrogen bond in the 2nd silicon oxide 22 is promoted by using N2O as a compound containing oxygen. Consequently, gasification components, such as moisture contained in the 2nd silicon oxide 22 and hydrogen, can be removed more certainly.
[0052] In consideration of the role which adjusts the thickness of the layer insulation film needed, and the function by which N2O plasma is desorbed from hydrogen bond, 100nm or more of thickness of this 3rd silicon oxide 24 is more preferably set as 100–600nm.
[0053] d. Perform annealing processing at the temperature of 600–850 degrees C in annealing processing, next nitrogen–gas–atmosphere mind. By this annealing processing, the 2nd silicon oxide 22 of the above and the 3rd silicon oxide 24 turn precisely, and have good insulation and good water resistance. That is, by setting an annealing temperature as 600 degrees C or more, the condensation polymerization reaction of the silanol in the 2nd silicon oxide 22 is performed nearly completely, and the water and hydrogen which are contained in this film are fully emitted, and can form a precise film. Moreover, by setting an annealing temperature as 850 degrees C or less, it cannot have bad influences, such as a punch through and junction leak, on the diffusion layer of the source field which constitutes an MOS transistor, or a drain field, and detailed–ization of an element can be attained.
[0054] In annealing processing, in order to make small influence of a heat strain to the 2nd silicon oxide 22, it is desirable to perform run ping annealing which raises the temperature of a wafer gradually or continuously. For example, when carrying out a temperature up to an annealing temperature (600–850 degrees C) after keeping a wafer warm at about 400 degrees C, high impurity concentration of the 3rd silicon oxide 24 can be made quite low. For example, when an impurity is Lynn, the gettering effect of mobile ion is set aside and the concentration of Lynn is checking that a crack does not arise in the 2nd silicon oxide 22 at least 2 or less % of the weight.

[0055] e. Form the 4th silicon oxide 26 of 1000–1500nm of thickness by the plasma CVD method at 350–400 degrees C using formation, next the 4th TEOS and oxygen of a silicon oxide 26.

[0056] Even when not performing annealing, the silicon oxide of the TEOS-oxygen using the plasma CVD method is of the same grade as the 2nd silicon oxide 22 of the above which carried out elevated-temperature annealing, and the 3rd silicon oxide 24, or has a somewhat quick dry etching speed. This becomes the factor which obtains the contact hole of a good configuration, without producing the vena contracta and a level difference on the hole side in formation of the contact hole mentioned later.
[0057] (C) Next, explain the process shown in drawing 1 (C).
[0058] (Smoothing by CMP) Subsequently, the 4th silicon oxide 26 of the above, and if needed, by the chemical machinery-grinding (CMP) method, predetermined thickness is ground and the 3rd silicon oxide 24 of the above and the 2nd silicon oxide 22 are smoothed. And the 2nd silicon oxide 22 of the above, the 3rd silicon oxide 24, and the 4th silicon oxide 26 can obtain a flat front face, though a part of 3rd silicon oxide 24 or 2nd silicon oxide 22 is exposed to a front face with polish, since polish speed is almost the same, therefore management of the amount of polishes is easy for them.
[0059] For example, according to research of this invention persons, the polish speed of each silicon oxide was as follows.
[0060]
The 2nd silicon oxide (800 degrees C of annealing temperatures) A part for;250nm/ The 3rd silicon oxide (800 degrees C of annealing temperatures) A part for;250nm/ The 4th silicon oxide (with no annealing) ; a part for 250nm/ BPSG film [for comparison] (900 degrees C of annealing temperatures); — the process shown in 350nm a part (D) for /next and drawing 2 (A) is explained — subsequently (formation of a contact hole) The contact hole 32 whose aperture is 0.2-0.5 micrometers is formed by carrying out anisotropic etching of the silicon oxides 20, 22, 24, and 26 which constitute the 1st layer insulation film I1 from a reactant ion etcher which made CHF3 and CF4 the main gas alternatively.
[0061] This contact hole 32 constitutes the shape of a taper to which aperture becomes small linearly toward a pars basilaris ossis occipitalis from the upper-limit section. Although the angle theta of a taper cannot generally be ******(ed) according to etching conditions etc., it has five - 15 inclinations, for example. As a reason the through hole of the shape of such a taper is obtained, silicon oxides 20, 22, 24, and 26 have the fundamental almost same etch rate, and the interface of each silicon oxide is [1st] further that the 2nd silicon oxide 22 has a slightly small etch rate compared with the 3rd silicon oxide 24, and the 2nd to have stuck very good. Within the contact hole 32 of the shape of such a taper, good deposition of an aluminum film is possible so that it may mention later.
[0062] The dry etching speed of each silicon oxide which invention-in-this-application persons measured below is indicated. In addition, dry etching was performed on condition that power;800W, atmospheric pressure;20Pa, and etchant gas;CF4:CHF3:helium=1:2:9.
[0063]
The 2nd silicon oxide (800 degrees C of annealing temperatures) A part for;525nm/ The 3rd silicon oxide (800 degrees C of annealing temperatures) A part for;550nm/ The 4th silicon oxide (with no annealing) A part for;565nm/ The BPSG film for comparison (900 degrees C of annealing temperatures); the process shown in 750nm a part (E) for /next and drawing 2 (B) is explained.
[0064] (Degasifying processing) ****** which includes a degasifying process first — it ****** just
[0065] By the lamp chamber, lamp heating for 30 - 60 seconds (heat treatment A) is given at the base pressure of 1.5x10 - 4 or less Pa, and the temperature of 150-250 degrees C. Subsequently, degasifying processing is performed by introducing argon gas by another chamber by the pressure of 1x10-1 to 15x10 to 1 Pa, and performing heat treatment for 30 - 120 seconds (degasifying process; heat treatment B) at the temperature of 150-550 degrees C.
[0066] In this process, the moisture adhering to the wafer etc. is removable by mainly heat-treating the whole wafer including the rear face and the side of a wafer in heat treatment A first.

[0067] Furthermore, in heat treatment B, the gasification component in the 2nd silicon oxide 22 which constitutes the 1st layer insulation film I1 (H, H2O) is mainly removable. Consequently,

generating of the gasification component from the 1st layer insulation film I1 can be prevented at the time of formation of the barrier layer of the following process, and an aluminum film.
[0068] The barrier layer 33 is constituted in the gestalt of this operation by the multilayer which consists of a barrier film which has barrier ability, and an electric conduction film. An electric conduction film is formed between a barrier film and an impurity diffusion layer, in order to raise conductivity with the impurity diffusion layer formed in the barrier film and the silicon substrate, i.e., a source field, and a drain field. As a barrier film, the common matter, for example, titanium night RAIDO and a titanium tungsten, can be used preferably. Moreover, refractory metals, such as titanium, cobalt, and a tungsten, can be used as an electric conduction film. These titanium, cobalt, and a tungsten react with the silicon which constitutes a substrate, and serve as silicide.
[0069] Since it dissolves the gasification component (O, H, H2 O, N) of dozens atom %, before a barrier layer, for example, a TiN film / Ti film, forms these films, it is very effective [film] to remove the gasification component in the 1st layer insulation film I1, when forming the aluminum film within a contact hole good. If the gasification component in the 1st [of the low rank of a barrier layer] layer insulation film I1 is not fully removed, at the temperature at the time of formation of a barrier layer (usually 300 degrees C or more), the gasification component in the 1st layer insulation film I1 will be emitted, and this gas will be incorporated in a barrier layer. Furthermore, in order that this gas may secede from a barrier layer at the time of membrane formation of an aluminum film and may come out to the interface of a barrier layer and an aluminum film, it has a bad influence on the adhesion of an aluminum film, or a fluidity.
[0070] (Membrane formation of a barrier layer) By the spatter, as an electric conduction film which constitutes the barrier layer 33, a titanium film is formed by 20–70nm thickness, and, subsequently a TiN film is formed as a barrier film by another chamber at 30–150nm thickness. The temperature of a spatter is chosen in 200–450 degrees C according to thickness.
[0071] Next, titanium oxide can be formed in the shape of an island into a barrier layer by exposing for 10 – 100 seconds into oxygen plasma by the pressure of 0.1x102 to 1.5x102Pa, and carrying out annealing processing over 10 – 60 minutes in 450–700–degree C nitrogen or hydrogen atmosphere. It is checking that the barrier property of a barrier layer can be raised by this processing.
[0072] Moreover, 400–800–degree C heat treatment in the lamp annealing furnace which contains hundreds of ppm – several% of oxygen at least can also perform this annealing processing, and the barrier property of a barrier layer can be raised similarly.
[0073] In addition, although illustration is not carried out, it is the purpose which raises the wettability to the aluminum film mentioned later, and the WETTENGU layer which consists of titanium, cobalt, silicon, etc. may be formed in the front face of the barrier layer 33. The 1st aluminum membrane fluidity can be raised by preparing such a WETTENGU layer. There should just usually be thickness dozens of nm or more of a WETTENGU layer.
[0074] (Degasifying processing before membrane formation of an aluminum film, and cooling of a wafer) First, before cooling a wafer, heat treatment for 30 – 60 seconds (heat treatment C) is performed in a lamp chamber at the base pressure of 1.5x10 – 4 or less Pa, and the temperature of 150–250 degrees C, and matter, such as water adhering to the substrate, is removed. Then, before forming an aluminum film, 100 degrees C or less of substrate temperature are preferably lowered to ordinary temperature –50 degree C temperature. This cooling process is important in order to lower the substrate temperature which rose with the above–mentioned heat treatment C, for example, on the stage which has a water–cooled function, lays a wafer and lowers this wafer temperature to predetermined temperature.
[0075] Thus, in case the 1st aluminum film is formed by cooling a wafer, the 1st layer insulation film I1 and the barrier layer 33, and capacity further emitted from the whole wafer surface can be lessened as much as possible. Consequently, the influence of gas detrimental to the coverage nature and adhesion which stick to the interface of the barrier layer 33 and the 1st aluminum film 34 can be prevented.
[0076] (Membrane formation of an aluminum film) First, it is 30–100 degrees C in temperature more preferably, and the aluminum containing 0.2 – 1.0% of the weight of copper is formed at high speed by the spatter by 150–300nm of thickness, and 200 degrees C or less of 1st aluminum film

34 are formed. Then, it heats in substrate temperature of 420–460 degrees C within the same chamber, the aluminum which contains copper similarly is formed by the low speed by the spatter, and the 2nd aluminum film 35 of 300–600nm of thickness is formed. Here, in membrane formation of an aluminum film, although neither membrane formation conditions nor the design matter of a device manufactured can prescribe "high speed" generally, a sputtering rate 10nm [/second] or more is meant about, and a "low speed" means a sputtering rate 3nm [/second] or less about.

[0077] An example of the sputtering system for forming the 1st and 2nd aluminum films 34 and 35 to drawing 6 is shown. This sputtering system has the electrode 52 which serves both as the target 51 which serves as an electrode in a chamber 50, and a stage, and it is constituted so that the substrate (wafer) W processed may be installed on an electrode 52. The 1st gas supply way 53 is connected to a chamber 50, and the 2nd gas supply way 54 is connected to the electrode 52. Argon gas is supplied from [each] the gas supply ways 53 and 54. And the temperature of Wafer W is controlled by the gas supplied from the 2nd gas supply way 54. In addition, the means for discharging the gas in a chamber 50 is not illustrated.

[0078] An example which controlled substrate temperature using such a sputtering system is shown in drawing 7 . In drawing 7 , a horizontal axis shows elapsed time and a vertical axis shows substrate (wafer) temperature. Moreover, in drawing 7 , the line which the line shown with Sign a shows the substrate temperature change when setting the temperature of the stage 52 of a sputtering system as 350 degrees C, and is shown with Sign b shows change of the substrate temperature when raising the temperature of a stage 52 by supplying hot argon gas in a chamber through the 2nd gas supply way 54.

[0079] For example, the temperature control of a substrate is performed as follows. First, the temperature of a stage 52 is beforehand set as the temperature (350–500 degrees C) for forming the 2nd aluminum film. In case the 1st aluminum film is formed, there is no supply of the gas from the 2nd gas supply way 54, and substrate temperature rises gradually by heating by the stage 52, as the sign a of drawing 7 shows. By supplying the gas heated through the 2nd gas supply way 54, in case the 2nd aluminum film is formed, substrate temperature rises rapidly and is controlled to become fixed at predetermined temperature so that the sign b of drawing 7 shows.

[0080] In the example shown in drawing 7 , stage temperature is set as 350 degrees C, while substrate temperature is set as 125–150 degrees C, the 1st aluminum film 34 is formed, and membrane formation of the 2nd aluminum film 35 is performed immediately after that.

[0081] In membrane formation of an aluminum film, control of the power impressed to a sputtering system with membrane formation speed and a substrate temperature control is also important. That is, although membrane formation speed is related, in case membrane formation of the 1st aluminum film 34 is performed by high power, the 2nd aluminum film 35 is performed by low power and it switches to low power from still higher power, it is important not to make power into zero. If power is made into zero, an oxide film will be formed in the bottom of reduced pressure on the front face of the 1st aluminum film, the wettability of the 2nd [to the 1st aluminum film] aluminum film will fall, and both adhesion will become bad. In other words, by always impressing power, supplying activity aluminum to the front face of the aluminum film under membrane formation can be continued, and formation of an oxide film can be suppressed. In addition, although the size of power cannot generally be specified depending on a sputtering system, membrane formation conditions, etc., in the case of the temperature conditions shown, for example in drawing 7 , it is desirable [a size] to set 5–10kW and low power as 300W–1kW for high power.

[0082] Thus, by forming continuously the 1st aluminum film 34 and the 2nd aluminum film 35 within the same chamber, control of temperature and power can be performed strictly and it becomes possible to form efficiently the aluminum film which is low temperature and was stabilized rather than before.

[0083] The thickness of the aluminum film 34 of the above 1st has desirable 200–400nm, for example, although the proper range is chosen from that a continuation layer can be formed and this aluminum film 34 by good step coverage in consideration of the ability to suppress discharge

of the gasification component from the lower layer barrier layer 33 and the 1st layer insulation film I1. Moreover, although the 2nd aluminum film 35 is determined by the size of a contact hole, its aspect ratio, etc., in order for an aspect ratio to fill a hole 0.5 micrometers or less about by three, for example, 300–1000nm thickness is required for it.
[0084] (Membrane formation of an antireflection film) The antireflection film 36 of 30–80nm of thickness is formed by depositing TiN by the spatter by still more nearly another spatter chamber. Then, the deposit which consists of the aforementioned barrier layer 33, the 1st aluminum film 34, the 2nd aluminum film 35, and an antireflection film 36 by the anisotropy dry etcher which makes the gas of Cl2 and BCl3 a subject is **********ed alternatively, and patterning of the 1st metal wiring layer 30 is performed.
[0085] Thus, in the formed metal wiring layer 30, it was checked that aluminum is embedded by good step coverage, without an aspect ratio generating a void in 0.5–3 in the contact hole whose aperture is 0.2–0.8 micrometers.
[0086] (F) Next, explain the process shown in drawing 3 (A).
[0087] (Formation of the 2nd layer insulation film I2) The 2nd layer insulation film I2 has the same composition as the layer insulation film I1 of the above 1st fundamentally. That is, the 2nd layer insulation film I2 consists of the 1st silicon oxide 70, the 2nd silicon oxide 72, the 3rd silicon oxide 74, and the 4th silicon oxide 76 in order of the silicon oxide of four layers, i.e., a lower shell. And these silicon oxides 70, 72, 74, and 76 are formed by the same method as the aforementioned silicon oxides 20, 22, 24, and 26 except annealing processing. Although main portions are explained below, a publication is omitted about a common matter.
[0088] a. **** of the 1st silicon oxide 70 — the 1st silicon oxide 70 of 50–200nm of thickness is first formed by making a tetrapod ethoxy run (TEOS) and oxygen react by the plasma–chemistry vapor–growth (CVD) method at 300–500 degrees C
[0089] b. Form the 2.5x102Pa or less of the 2nd silicon oxide 72 preferably formation of the 2nd silicon oxide 72, next by making SiH4 and H2O2 react by CVD at the temperature of 0–10 degrees C by using nitrogen gas as a carrier more preferably under reduced pressure of 0.3x102 to 2.0x102Pa. The 2nd silicon oxide 72 is formed by the thickness which has larger thickness than the level difference of the 1st lower layer silicon oxide 70 at least, that is, fully covers this level difference like the 2nd silicon oxide 22 of the above. Moreover, the upper limit of the thickness of the 2nd silicon oxide 72 is set as the grade which a crack does not produce in this film. Specifically, in order to obtain better flat nature, as for the thickness of the 2nd silicon oxide 72, it is desirable that it is thicker than a lower layer level difference, and it is preferably set as 500–1000nm.
[0090] 0–20 degrees C of membrane formation temperature of the 2nd silicon oxide 72 are more preferably set as 0–10 degrees C.
[0091] The 2nd silicon oxide 72 formed at this process has a high fluidity, and is excellent in a flattening property.
[0092] c. The PSG film (the 3rd silicon oxide) 74 of 100–600nm of thickness is formed by making it react to the bottom of existence of formation of the 3rd silicon oxide 74 next SiH4 and PH3, and N2O by the plasma CVD method at the temperature of 300–450 degrees C at 200–600kHz high frequency.
[0093] Moreover, the 3rd silicon oxide 74 needs that desorption of gasification components, such as water contained in the 2nd silicon oxide 72 of the above like the 3rd silicon oxide 24 of the above by the annealing processing performed behind, is easy, and to be porous (porosity) in consideration of fully being carried out. For that purpose, temperature is desirable and it is preferably [more] desirable [the 3rd silicon oxide 74] 1MHz or less preferably to form membranes by the 200–600kHz RF plasma CVD method more preferably, and to contain impurities, such as Lynn, 300–400 degrees C 450 degrees C or less. By containing such an impurity in the 3rd silicon oxide 74, the 3rd silicon oxide 74 will be in a more nearly porous state, and can ease the stress to a film. The concentration of such an impurity is set up in consideration of points, such as stress–proof nature and the gettering effect. For example, when an impurity is Lynn, it is desirable to be contained at 1 – 6% of the weight of a rate.
[0094] Moreover, in plasma CVD, desorption of the hydrogen bond in the 2nd silicon oxide 72 is

promoted by using N2O as a compound containing oxygen. Consequently, gasification components, such as moisture contained in the 2nd silicon oxide 72, can be removed more certainly.
[0095] 100nm or more of thickness of this 3rd silicon oxide 74 is more preferably set as 200–600nm.
[0096] d. Perform annealing processing at annealing processing, next the temperature of 350–500 degrees C. By this annealing processing, the 2nd silicon oxide 72 of the above and the 3rd silicon oxide 74 turn precisely, and have good insulation and good water resistance. That is, by setting an annealing temperature as 350 degrees C or more, the condensation polymerization reaction of the silanol in the 2nd silicon oxide 72 is performed nearly completely, and the moisture contained in this film is fully emitted, and can form a precise film. Moreover, it does not have a bad influence on the aluminum film which constitutes the 1st wiring layer 40 by setting an annealing temperature as 500 degrees C or less.
[0097] e. Form the 4th silicon oxide 76 of 1000–1500nm of thickness by the plasma CVD method at 350–400 degrees C using formation, next the 4th TEOS and oxygen of a silicon oxide 76.
[0098] (G) Next, explain the process shown in drawing 3 (B).
[0099] (Smoothing by CMP) The 3rd silicon oxide 74 of the above and the 2nd silicon oxide 72 are ground and smoothed by predetermined thickness by the CMP method the 4th silicon oxide 76 of the above, and if needed. By this data smoothing, though a part of 3rd silicon oxide 74 or 2nd silicon oxide 72 is exposed to a front face with polish, a flat front face can be obtained, therefore management of the amount of polishes is easy.
[0100] (H) Next, explain the process shown in drawing 4 (A).
[0101] (Formation of a beer hall) By carrying out anisotropic etching of the 2nd layer insulation film I2 and antireflection film 36 alternatively by the reactant ion etcher which made CHF3 and CF4 the main gas, the beer hall 62 whose aperture is 0.3–0.5 micrometers is formed.
[0102] This beer hall 62 constitutes the shape of a taper to which aperture becomes small gradually toward a bottom from the upper–limit section like the aforementioned contact hole 32. Although the angle theta of a taper cannot generally be ******(ed) according to etching conditions etc., it has five – 15 inclinations, for example.
[0103] (I) Next, the process shown in drawing 4 (B) is explained.
[0104] (Degasifying processing) ****** which includes a degasifying process first — it ****** just
[0105] By the lamp chamber, lamp heating for 30 – 60 seconds (heat treatment D) is given at the base pressure of 1.5x10 – 4 or less Pa, and the temperature of 150–250 degrees C. Subsequently, degasifying processing is performed by introducing argon gas by another chamber by the pressure of 1x10–1 to 15x10 to 1 Pa, and performing heat treatment for 30 – 120 seconds (degasifying process; heat treatment E) at the temperature of 300–500 degrees C.
[0106] In this process, the moisture adhering to the wafer etc. is removable by mainly heat–treating the whole wafer including the rear face and the side of a wafer in heat treatment D first.

[0107] Furthermore, in heat treatment E, the gasification component in the 2nd layer insulation film I2 (H, H2O) is mainly removable. Consequently, generating of the gasification component from the 2nd layer insulation film I2 can be prevented at the time of formation of the WETTENGU layer of the following process, and an aluminum film.
[0108] In the gestalt of this operation, since it dissolves the gasification component (O, H, H2 O, N) of dozens atom %, before a WETTENGU layer, for example, Ti film, forms this film, it is very effective [film] to remove the gasification component in the 2nd layer insulation film I2, when forming th aluminum film in a beer hall good. If the gasification component in the 2nd [of the low rank of a WETTENGU layer] layer insulation film I2 is not fully removed, the gasification component in the 2nd layer insulation film I2 will be emitted at the time of formation of a WETTENGU layer, and this gas will be incorporated in a WETTENGU layer at it. Furthermore, in order that this gas may secede from a WETTENGU layer at the time of membrane formation of an aluminum film and may come out to the interface of a WETTENGU layer and an aluminum film, it has a bad influence on the adhesion of an aluminum film, or a fluidity.

[0109] (Membrane formation of a WETTENGU layer) By the spatter, a titanium film is formed by 20-70nm thickness as a film which constitutes the WETTENGU layer 63. 100 degrees C or less of temperature of a spatter are 25 degrees C or less more preferably.
[0110] (Cooling of the wafer before membrane formation of an aluminum film) Before forming an aluminum film, 100 degrees C or less of substrate temperature are preferably lowered to ordinary temperature -50 degree C temperature. This cooling process is important in order to lower the substrate temperature which rose by the spatter of the WETTENGU layer 63, for example, on the stage which has a water-cooled function, lays a wafer and lowers this wafer temperature to predetermined temperature.
[0111] Thus, in case the 1st aluminum film is formed by cooling a wafer, the 2nd layer insulation film I2 and the WETTENGU layer 63, and capacity further emitted from the whole wafer surface can be lessened as much as possible. Consequently, the influence of gas detrimental to the coverage nature and adhesion which stick to the interface of the WETTENGU layer 63 and the 1st aluminum film 64 can be prevented.
[0112] (Membrane formation of an aluminum film) First, it is 30-100 degrees C in temperatur more preferably, and the aluminum containing 0.2 - 1.0% of the weight of copper is formed at high speed by the spatter by 150-300nm of thickness, and 200 degrees C or less of 1st aluminum film 64 are formed. Then, it heats in substrate temperature of 420-460 degrees C within the same chamber, the aluminum which contains copper similarly is formed by the low speed by the spatter, and the 2nd aluminum film 65 of 300-600nm of thickness is formed.
[0113] The thing same as a sputtering system as the equipment shown in drawing 6 can be used. About the composition of the aforementioned sputtering system, the temperature control of a wafer, and the power at the time of a spatter, since it is the same as that of the case of the 1st metal wiring layer 30, detailed explanation is omitted.
[0114] By forming continuously the 1st aluminum film 64 and the 2nd aluminum film 65 within the same chamber, control of temperature and power can be performed strictly and it becomes possible to form efficiently the aluminum film which is low temperature and was stabilized rather than before.
[0115] The thickness of the aluminum film 64 of the above 1st has desirable 100-300nm, for example, although the proper range is chosen from that a continuation layer can be formed and this aluminum film 64 by good step coverage in consideration of the ability to suppress discharge of the gasification component from the lower layer WETTENGU layer 63 and the 2nd layer insulation film I2. Moreover, although the 2nd aluminum film 65 is determined by the size of a beer hall 62, its aspect ratio, etc., in order for an aspect ratio to fill a hole 0.5 micrometers or less about by three, for example, 300-800nm thickness is required for it.
[0116] (Membrane formation of an antireflection film) The antireflection film 66 of 30-80nm of thickness is formed by depositing TiN by the spatter by still more nearly another spatter chamber. Then, the deposit which consists of the aforementioned WETTENGU layer 63, the 1st aluminum film 64, the 2nd aluminum film 65, and an antireflection film 66 by the anisotropy dry etcher which makes the gas of Cl2 and BCl3 a subject is **********ed alternatively, and patterning of the 2nd metal wiring layer 60 is performed.
[0117] Thus, in the formed metal wiring layer 60, it was checked that aluminum is embedded by good step coverage, without an aspect ratio generating a void in 0.5-3 in the beer hall whose aperture is 0.2-0.8 micrometers.
[0118] Henceforth, it is the 3rd and the 4th like the 2nd wiring field L2 if needed. — A multilayer-interconnection field can be formed.
[0119] (J) Next, explain the process shown in drawing 5 .
[0120] (Formation of the protection insulator layer PL) The protection insulator layer PL consists of the 1st silicon oxide 80, the 2nd silicon oxide 82 and the 3rd silicon oxide 84, and a silicon nitride 86 in order of the silicon oxide of three layers, i.e., a lower shell. And these silicon oxides 80, 82, and 84 are formed by the same method as the aforementioned silicon oxides 20, 22, and 24 except annealing processing. Although main portions are explained below, a publication is omitted about a common matter. Moreover, the silicon oxide which does not include Lynn is sufficient as the 3rd silicon oxide 84.

[0121] a. **** of the 1st silicon oxide 80 — the 1st silicon oxide 80 of 50–500nm of thickness is first formed by making a tetrapod ethoxy run (TEOS) and oxygen react by the plasma-chemistry vapor-growth (CVD) method at 300–500 degrees C
[0122] b. Form the 2.5x102Pa or less of the 2nd silicon oxide 82 preferably formation of the 2nd silicon oxide 82, next by making SiH4 and H2O2 react by CVD at the temperature of 0–10 degrees C by using nitrogen gas as a carrier more preferably under reduced pressure of 0.3x102 to 2.0x102Pa. The 2nd silicon oxide 82 is formed by the thickness which has larger thickness than the level difference of the 1st lower layer silicon oxide 80 at least, that is, fully covers this level difference like the 2nd silicon oxide 22 of the above. Moreover, the upper limit of the thickness of the 2nd silicon oxide 82 is set as the grade which a crack does not produce in this film. Specifically, in order to obtain better flat nature, as for the thickness of the 2nd silicon oxide 82, it is desirable that it is thicker than a lower layer level difference, and it is preferably set as 500–1000nm.
[0123] 0–20 degrees C of membrane formation temperature of the 2nd silicon oxide 82 are more preferably set as 0–10 degrees C.
[0124] The 2nd silicon oxide 82 formed at this process has a high fluidity, and is excellent in a flattening property.
[0125] c. The 3rd silicon oxide 84 is formed by making it react to the bottom of existence of formation of the 3rd silicon oxide 84 next SiH4, and N2O by the plasma CVD method at the temperature of 300–450 degrees C at 200–600kHz high frequency.
[0126] Moreover, the 3rd silicon oxide 84 needs that desorption of gasification components, such as water contained in the 2nd silicon oxide 82 of the above like the 3rd silicon oxide 24 of the above by the annealing processing performed behind, is easy, and to be porous (porosity) in consideration of fully being carried out. For that purpose, temperature is desirable and, as for the 3rd silicon oxide 84, it is desirable for 450 degrees C or less to be the PSG film with which membranes are more preferably formed by 300–400 degrees C 1MHz or less by the 200–600kHz RF plasma CVD method more preferably, and impurities, such as Lynn, are contained by introduction of PH3 gas etc. By containing such an impurity in the 3rd silicon oxide 84, the 3rd silicon oxide 84 will be in a more nearly porous state, and can ease the stress to a film. The concentration of such an impurity is set up in consideration of points, such as stress-proof nature and the gettering effect. For example, when an impurity is Lynn, it is desirable to be contained at 1 – 6% of the weight of a rate.
[0127] Moreover, in plasma CVD, desorption of the hydrogen bond in the 2nd silicon oxide 82 is promoted by using N2O as a compound containing oxygen. Consequently, gasification components, such as moisture contained in the 2nd silicon oxide 82, can be removed more certainly.
[0128] 100nm or more of thickness of this 3rd silicon oxide 84 is more preferably set as 200–600nm.
[0129] d. Perform annealing processing at annealing processing, next the temperature of 350–500 degrees C. By this annealing processing, the 2nd silicon oxide 82 of the above and the 3rd silicon oxide 84 turn precisely, and have good insulation and good water resistance. That is, by setting an annealing temperature as 350 degrees C or more, the condensation polymerization reaction of the silanol in the 2nd silicon oxide 82 is performed nearly completely, and the moisture contained in this film is fully emitted, and can form a precise film. Moreover, it does not have a bad influence on the aluminum film which constitutes the 2nd wiring layer 60 by setting an annealing temperature as 500 degrees C or less.
[0130] e. Form the silicon nitride 86 of the best layer by making SiH4 and NH3 react by the plasma CVD method at the temperature of 300–450 degrees C by using formation, next the nitrogen gas of the silicon nitride 86 as a carrier. This silicon nitride 86 has 300–1500nm thickness in consideration of sufficient passivation function.
[0131] Then, the aforementioned protection insulator layer PL is alternatively **********ed on a mask by dry etching or wet etching in the photoresist which is not illustrated, and the hole for constituting the bonding putt section for external electrode ejection is formed. Moreover, in order to accept the need and to ease the stress at the time of the resin mould of a

semiconductor device, you may carry out the laminating of the films, such as polyimide resin, further.

[0132] In the form of this operation, since flattening is highly attained by the 1st silicon oxide 80 and the 2nd silicon oxide 82, the silicon nitride 86 which has a passivation function can constitute the protection insulator layer PL which was attached, and the surroundings were often evenly formed, and thickness did not produce a thin portion or a thin defect locally, and was excellent in moisture resistance or resistance to contamination. Furthermore, in the aforementioned protection insulator layer PL, in the 2nd metal wiring layer 60, since the film of a silicon oxide with a dielectric constant smaller than a silicon nitride exists between the adjoining metal wiring layers 60a and 60b, contribution of the capacity in a direction (horizontal) parallel to the front face of a silicon substrate 11 can be performed small. Therefore, electrical properties, such as a working speed of an element, can be raised compared with the structure where a silicon nitride with a high dielectric constant exists between metal wiring layers.

[0133] moreover, the 2nd silicon oxide 82 formed of the polycondensation reaction of a silicon compound and a hydrogen peroxide and the silicon oxides 80 and 84 of the 1st and 3 formed of plasma CVD have an etch rate of the same grade, as mentioned above — etc. — since it has the almost same etching property, the simple wet etching by mixed acids, such as HF and NH4F, is applicable not to mention dry etching

[0134] In addition, as a film equivalent to the 2nd silicon oxide 82, when for example, an SOG film is used, since the etch rate of an SOG film is large, side etching progresses, and there is a problem which a chipping and a crack tend to generate on the film above this SOG film.

[0135] In the gestalt of this operation, the following things can be considered as a reason for having the flat nature the protection insulator layer PL excelled [nature] in the 1st and the 2nd layer insulation film I1, and I2 row.

[0136] That is, since the resultant containing a silanol formed of the reaction of a silicon compound and a hydrogen peroxide has a high fluidity, when the irregularity on the front face of a wafer forms these films, flattening of the 2nd silicon oxide 22, 72, and 82 formed at the process shown in drawing 1 (B), drawing 3 (A), and drawing 5 is carried out highly.

[0137] Moreover, in the gestalt of this operation, the following things can be considered as a reason the 1st and 2nd aluminum films 64 and 65 were embedded by the contact hole 32 and the beer hall 62 on the 1st and 2nd aluminum films 34, and were embedded by fitness in 35 rows, respectively.

[0138] (a) By gasifying water and nitrogen which are contained in the insulator layers I1 and I2 between each class by performing a degasifying process, and fully emitting In the 1st subsequent aluminum film 34 and 64 and membrane formation of the 2nd aluminum 35 and 65, by preventing generating of the gas from the layer insulation films I1 and I2, the barrier layer 33, or the WETTENGU layer 63 Raised the adhesion of the WETTENGU layer 63 and the 1st aluminum film 64 to the barrier layer 33, the 1st aluminum film 34, and the row, and membrane formation of good step coverage was possible for.

[0139] (b) what the adhesion of the 1st aluminum film 34 and 64 was raised for in addition to the effect of the aforementioned degasifying process as the moisture or nitrogen which are contained in the WETTENGU layer 63 in substrate temperature at the layer insulation films I1 and I2 and barrier layer 33 row 200 degrees C or less by setting it as low temperature comparatively were not made to emit in membrane formation of the 1st aluminum film 34 and 64

[0140] (c) Since the 1st aluminum film 34 and 64 the very thing play further the role which suppresses generating of the gas from a lower layer when substrate temperature goes up, the 2nd following aluminum film 35 and 65 can be formed at comparatively high temperature, and flow diffusion of the 2nd aluminum film can be performed good.

[0141] (Semiconductor device) The semiconductor device (refer to drawing 5) applied to the gestalt of this operation by the above method can be formed. This semiconductor device has the 1st wiring field L1 formed on the silicon substrate 11 which contains the MOS device at least, and the aforementioned silicon substrate 11. The wiring field L1 of the above 1st is formed on the 1st silicon oxide 20 used as a base layer, the 2nd silicon oxide 22 formed of the polycondensation reaction of a silicon compound and a hydrogen peroxide, and the 2nd silicon

oxide 22 of the above. It is formed on the 3rd silicon oxide 24 containing impurities, such as Lynn, and the 3rd silicon oxide 24 of the above. By CMP Were formed on the barrier layer 33 formed in the front face of the contact hole 32 formed in the 1st layer insulation film I1 which consists of the 4th silicon oxide 26 by which flattening was carried out, and the aforementioned layer insulation film I1, the aforementioned layer insulation film I1, and the aforementioned contact hole 32, and the aforementioned barrier layer 33. It has the aluminum films 34 and 35 which consist of an alloy which makes aluminum or aluminum a principal component. And the aforementioned aluminum film 34 is connected to the titanium silicide layer 19 through the barrier layer 33.

[0142] The 2nd wiring field L2 formed on the wiring field L1 of the above 1st It is formed on the 1st silicon oxide 70 used as a base layer, the 2nd silicon oxide 72 formed of the polycondensation reaction of a silicon compound and a hydrogen peroxide, and the 2nd silicon oxide 72 of the above. It is formed on the 3rd silicon oxide 74 containing impurities, such as Lynn, and the 3rd silicon oxide 74 of the above. By CMP Were formed on the WETTENGU layer 63 formed in the front face of the beer hall 62 formed in the 2nd layer insulation film I2 which consists of the 4th silicon oxide 76 by which flattening was carried out, and the aforementioned layer insulation film I2, the aforementioned layer insulation film I2, and the aforementioned beer hall 62, and the aforementioned WETTENGU layer 63. It has the aluminum films 64 and 65 which consist of an alloy which makes aluminum or aluminum a principal component.

[0143] The protection insulator layer PL formed on the wiring field L2 of the above 2nd is formed the 1st silicon oxide 80 used as a base layer, the 2nd silicon oxide 82 formed of the polycondensation reaction of a silicon compound and a hydrogen peroxide, and on this 2nd silicon oxide 82, and has the 3rd silicon oxide 84 containing impurities, such as Lynn, and the silicon nitride 86 formed on this 3rd silicon oxide 84.

[0144] As mentioned above, according to the gestalt of this operation, the layer insulation films I1 and I2 and the protection insulator layer PL which have very good flat nature can be formed by forming the silicon oxide containing ****** of a silanol obtained according to the gaseous phase reaction of a silicon compound and a hydrogen peroxide.

[0145] And since the 1st layer insulation film I1 can be formed at remarkable low temperature compared with the conventional BPSG film, it can improve a property in respect of a punch through, junction leak, etc., therefore can attain detailed-izing of an element, and reliable contact structure, and its manufacture process top is also advantageous.

[0146] Moreover, since it has flat nature with the advanced layer insulation films I1 and I2, a process margin including processing of a wiring layer etc. can be made to be able to increase, and quality and the yield can be raised.

[0147] Furthermore, it not only can form the silicon nitride 86 which has a high passivation function, but in the protection insulator layer PL, from having the 2nd silicon oxide 82 which was excellent in flat nature, there are few defects at uniform thickness and reduction of a mutual capacity of the metal wiring layer of the same layer can attain improvement in an electrical property.

[0148] Moreover, in the gestalt of this operation, by forming an aluminum film continuously [it is still more desirable and] within the same chamber including a degasifying process and a cooling process at least before the spatter of an aluminum film, it became possible to embed the contact hole and beer hall to about 0.2 micrometers only by aluminum or the aluminium alloy, and improvement was able to be aimed at in respect of reliability and the yield. Moreover, there are also no copper segregation and unusual growth of crystal grain in the aluminum film which constitutes the contact section, and the good thing was checked also in respect of reliability including migration etc.

[0149] (others — gestalt of operation) this invention is not limited to the gestalt of the above-mentioned implementation, but can replace the part with the following meanses

[0150] (a) In the gestalt of the aforementioned implementation, although the dinitrogen oxide was used as a compound containing oxygen at the time of membrane formation by the plasma CVD of the 3rd silicon oxide 24, 74, and 84 instead, ozone can also be used. And before forming the 3rd silicon oxide 24, 74, and 84, it is desirable to expose a wafer to ozone atmosphere.

[0151] For example, Wafer W is laid and it is made to move at the rate of predetermined using the belt furnace shown in drawing 8 onto the conveyance belt 80 heated by 400–500 degrees C at the heater 82. At this time, ozone is supplied from 1st gas head 86a, and the aforementioned wafer W is passed for the inside of 2 – 8% of the weight of ozone atmosphere over the time for 5 minutes or more. Subsequently, ozone, TEOS, and TMP (P(OCH3) 3) are mostly supplied by the ordinary pressure from the 2nd and 3rd gas heads 86b and 86c, and the PSG films (the 3rd silicon oxide) 24, 74, and 84 whose concentration of Lynn is 3 – 6 % of the weight are formed by 100–600nm of thickness. In addition, in drawing 8 , a sign 84 shows covering.
[0152] Thus, by using ozone instead of a dinitrogen oxide, the silicon oxide by TEOS can be formed by the ordinary pressure CVD. Moreover, membranes can be continuously formed efficiently by using a belt furnace.
[0153] By exposing Wafer W into ozone atmosphere, moreover, by the thermal–desorption spectrum (TDS) and the infrared spectroscopy (FTIR) The 2nd silicon oxide 22, 72, and 82 has enough little hygroscopicity and moisture, It was checked that the flat nature of the layer insulation films I1 and I2 is good like the case where a dinitrogen oxide is used as reactant gas, that the property of an MOS transistor is good, and that a crack does not occur in the 2nd silicon oxide 22, 72, and 82.
[0154] (b) With the gestalt of the aforementioned implementation, although the silicon oxide using TEOS by plasma CVD was used as the 1st silicon oxide 20, you may use a silicon oxide besides instead of for this. For example, the film formed by the reduced pressure heat CVD using the mono silane and the dinitrogen oxide as such 1st silicon oxide is sufficient. Membranes are faithfully formed to the shape of surface type of a lower layer silicon substrate, and not only coverage nature is good, but since this silicon oxide is precise, even if a passivation function is high and carries out the temperature up of it rapidly in annealing processing further, a crack cannot generate it easily in the 2nd silicon oxide 22. Moreover, in order to use heat CVD, there is an advantage without a plasma damage.
[0155] However, since it is necessary to set wafer temperature as about 750–800 degrees C in case membranes are formed by this method, it cannot be used on the film which is easy to oxidize like titanium silicide as Salicide structure, but it is necessary to use tungsten silicide or molybdenum silicide.
[0156] (c) With the gestalt of the aforementioned implementation, although the 1st layer insulation film I1 consists of silicon oxides of four layers, it may add not only this but other silicon oxides. For example, you may form the PSG film (concentration [of Lynn]; 1 – 6 % of the weight) of 100–300nm of thickness formed by the plasma CVD method between the 1st silicon oxide 20 and the 2nd silicon oxide 22. By putting in this PSG film, it was checked that the gettering function of a movable ion improves further and the threshold property of a transistor and change of the quiescent current decrease.
[0157] (d) With the gestalt of the aforementioned implementation, although the protection insulator layer PL contains the 3rd silicon oxide 84, it may be the composition except this silicon oxide 84.
[0158] In addition, although the gestalt of the above–mentioned implementation described the semiconductor device including a two–layer wiring field, this invention is applicable to the semiconductor device containing various kinds of elements, such as not only the semiconductor device that can apply also to the semiconductor device which, of course, includes the wiring field of three or more layers, and contains the N channel type MOS device but a P channel type or a CMOS type element. Furthermore, with the gestalt of the above–mentioned implementation, although flattening of the 4th silicon oxide 26 and 76 of the layer insulation films I1 and I2 was carried out by CMP, since it has the flat nature excellent in the 2nd silicon oxide 22 and 72, it is not necessary to necessarily establish this process.
[0159]

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (A), (B), and (C) are the cross sections showing typically an example of the manufacture method of the semiconductor device of this invention in order of a process.
[Drawing 2] (A) And (B) is the cross section showing typically an example of the manufacture method of the semiconductor device performed following the process shown in drawing 1 in order of a process.
[Drawing 3] (A) And (B) is the cross section showing typically an example of the manufacture method of the semiconductor device performed following the process shown in drawing 2 in order of a process.
[Drawing 4] (A) And (B) is the cross section showing typically an example of the manufacture method of the semiconductor device performed following the process shown in drawing 3 in order of a process.
[Drawing 5] It is the cross section showing an example in the manufacture method of the semiconductor device performed about the process shown in drawing 4 typically.
[Drawing 6] It is drawing showing typically an example of the sputtering system used for the gestalt of operation concerning this invention.
[Drawing 7] It is drawing showing the relation of the time and substrate temperature when controlling substrate temperature using the sputtering system shown in drawing 5 .
[Drawing 8] It is drawing showing typically the belt furnace used for manufacture of a semiconductor device.
[Description of Notations]
11 Silicon Substrate
12 Field Insulator Layer
13 Gate Oxide Film
14 Gate Electrode
15 Low Concentration Impurity Layer
16 High Concentration Impurity Layer
17 Side-Attachment-Wall Spacer
18 Silicon Oxide
19 Titanium Silicide Layer
20 1st Silicon Oxide
22 2nd Silicon Oxide
24 3rd Silicon Oxide
26 4th Silicon Oxide
32 Contact Hole
33 Barrier Layer
34 1st Aluminum Film
35 2nd Aluminum Film
62 Beer Hall
63 WETTENGU Layer
64 1st Aluminum Film

65 2nd Aluminum Film
70 1st Silicon Oxide
72 2nd Silicon Oxide
74 3rd Silicon Oxide
76 4th Silicon Oxide
80 1st Silicon Oxide
82 2nd Silicon Oxide
84 3rd Silicon Oxide
86 Silicon Nitride
I1, I2 Layer insulation film
PL Protection insulator layer
L1, L2 Wiring field

[Translation done.]